Power MOSFET Design in Load Switch

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Introduction

In portable electronic equipments such as cellular phones, laptops, and personal organizers, the claim for more features contradicts the battery using time. The solution to this problem is to turn off these elements when they are not being used. The circuit to turn off elements is referred to as a load switch. The application is shown in Fig. 1. Load switches are placed in series with the voltage source and the load. The typical load switch shows in Fig. 2.

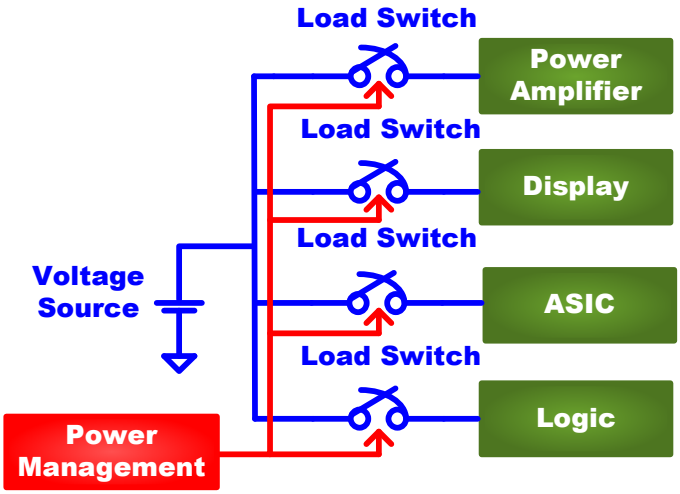

Fig. 1. A block diagram of a typical battery-powered application using load switches.

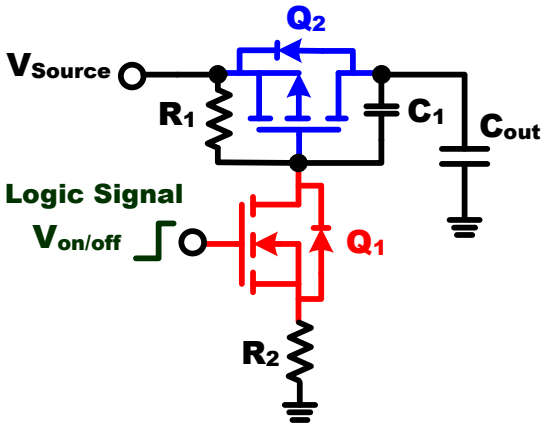

Fig. 2 A typical load switch schematic.

Load Switch Operation

A typical load switch uses p-channel MOSFET (Q2) with an n-channel MOSFET (Q1) gate driver. When the logic signal is “High”, the n-channel MOSFET (Q1) turns on and the p-channel MOSFET (Q2) also turns on, and the output voltage climbs to Vsource. When the logic signal is “Low”, the n-channel MOSFET and p-channel MOSFET both turn off, and the output is zero. With fast switching speed of today’s power MOSFET, the switch circuit turns in the short interval. In the initial turn on, the load voltage increases in a very high dV/dt speed which could induce high-peak inrush current at the output. The inrush current could far exceed the device rating and damage the semiconductor devices. The inrush current can be given by:

$$I_{inrush} = C_{out} \times \frac{dV}{dt} \quad (1)$$

There are two ways to reduce the inrush current; one is to slow down the transient speed of the logic signal, and another is adding a capacitor (C1) and a resistor (R2). When a high dV/dt appears at the output, a high induced current of the capacitor (C1) flows through n-channel MOSFET (Q1) to the resistor (R2). With the voltage crossing the resistor (R2) increase, the Vgs voltage of n-channel MOSFET (Q1) starts to reduce, and the dV/dt rate is pulled down. The resistor (R1) is to turn off the p-channel MOSFET (Q2).

Energy Consideration

The load switch circuits regarded as energy transformation. Energy transforms from a voltage source via MOSFET to a load capacitor. In the MOSFET design, the destruction can happen due to thermal overstress; the destruction is not because the current can not be handled, but the temperature of MOSFET excesses the limitation. The current direction shows in Fig. 3, and the capacitor voltage and current waveform shows in Fig. 4. The formula (2) is the capacitor voltage, and the formula (3) is the capacitor current.

$$V_C(t) = V_{IN}(1 - e^{\frac{-t}{R_{DS}C_{out}}}) \quad (2)$$

$$I_C(t) = \frac{V_{IN} - V_{IN}(1 - e^{\frac{-t}{R_{DS}C_{out}}})}{R_{DS(on)}} \quad (3)$$

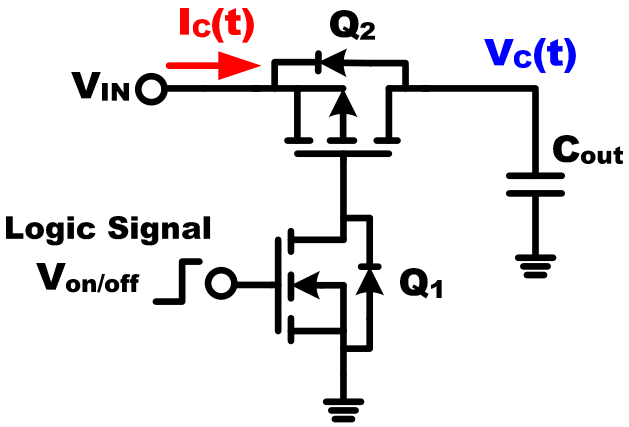

Fig. 3. The current direction.

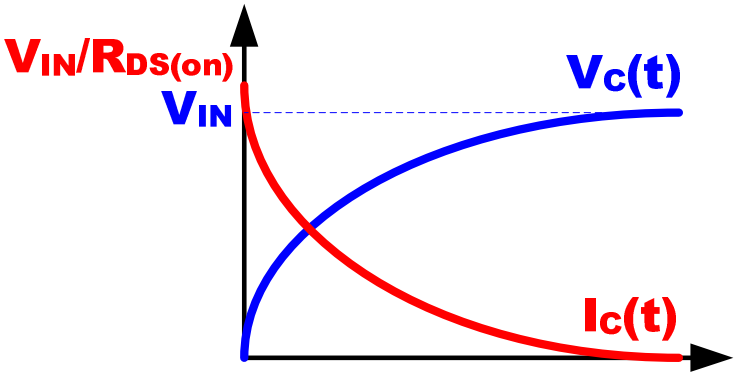

Fig. 4. The capacitor voltage and current waveform

The total energy transforms from source voltage to the output capacitor during the capacitor charging interval can be calculated in the formula (4). The power consumption during the capacitor charging interval can be calculated in the formula (6). There are some suppositions assumed in this paper: the rising time of MOSFET is neglected, the time charging the capacitor to V_{IN} is assumed $5R_{DS}C_{out}$, and the ESR of the output capacitor is very small enough to neglect.

$$E_{LS} = \int_0^{5R_{DS}Cout} V_C(t) \times I_C(t) \quad dt \tag{4}$$

$$\Rightarrow E_{LS} = \int_0^{5R_{DS}Cout} \frac{V_{IN}^2}{R_{DS}} e^{\frac{-t}{R_{DS}Cout}} \quad dt$$

$$\Rightarrow E_{LS} = \frac{V_{IN}^2 \times Cout}{2} \times (1 - e^{-10}) \tag{5}$$

$$P_{AV} = \frac{E_{LS}}{5R_{DS}Cout} = \frac{V_{IN}^2}{10R_{DS}}(1 - e^{-10}) \approx \frac{V_{IN}^2}{10R_{DS}} \tag{6}$$

This power causes an increase in junction temperature up to T_{JMAX}. The junction temperature of the p-channel MOSFET can be calculated by formula (6).

$$T_{Juction} = P_{AV} \times r(t) \times R_{\theta jc} + T_{Ambience} \tag{7}$$

where r(t) is the normalized effective transient thermal resistance, $R_{\theta jc}$ is the thermal resistance form junction to case, and $T_{Ambience}$ is the ambience temperature.
For example, NIKO-SEM's p-channel MOSFET P2003EV8 with 20mΩ on-state resistance, and 25 ℃/W junction-to-case thermal resistance is used in the load switch circuit, the source voltage is 10V, and ambience temperature is 26℃. If the capacitor is 2000μF, the junction temperature can be calculated as shown below:

- The time constant $5R_{DS}C_{out} = 5 \times 0.02 \times 2000\mu = 200\mu$
- The average power of p-channel MOSFET $P_{AV} = \frac{V_{IN}^2}{10R_{DS}} = \frac{100}{0.2} = 500$
- The normalized effective transient thermal resistance is 0.01 shown in Fig. 5.
- The junction temperature of P2003EV8 $T_{Juction} = 500 \times 0.01 \times 25 + 26 = 151$ ℃

This temperature excesses the maximum temperature T_{JMAX} which is 150℃. It means that the output capacitor muse be reduced, or MOSFET is replaced by less R_{DS}. The charging time of different values of capacitors is shown in Fig. 6. To charging larger capacitor needs longer time, and the power consumption of the p-channel MOSFET also increases. If using less R_{DS} MOSFET, the peak current and the charging time can both reduce, and the power consumption can decrease.

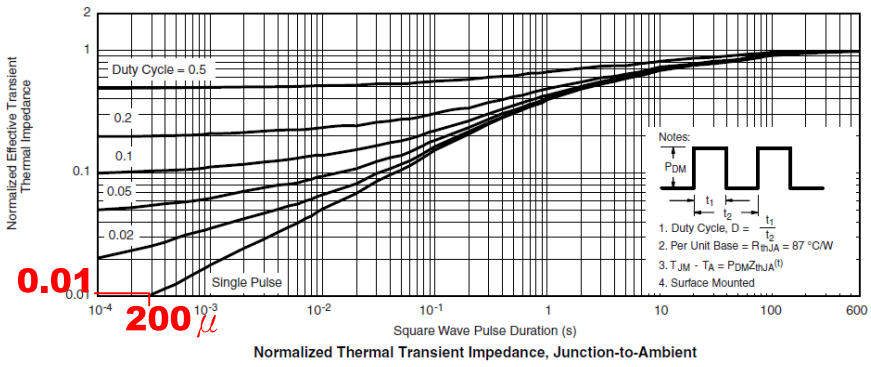

Fig. 5. Maximum effective transient thermal impedance plot, junction to case

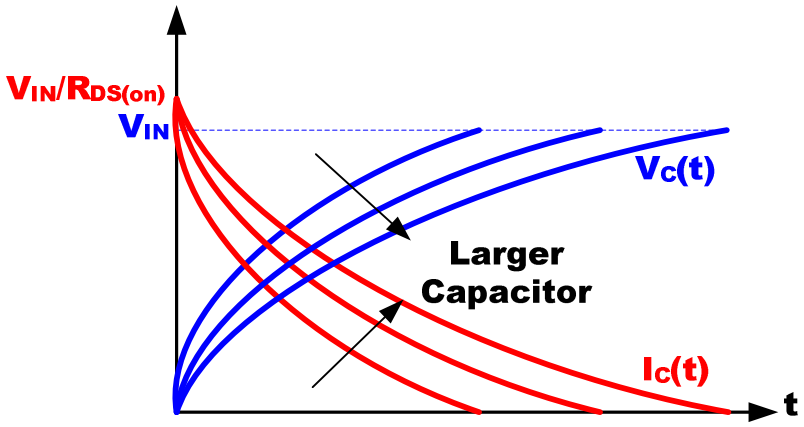

Fig. 6. Various capacitor values Vs. time

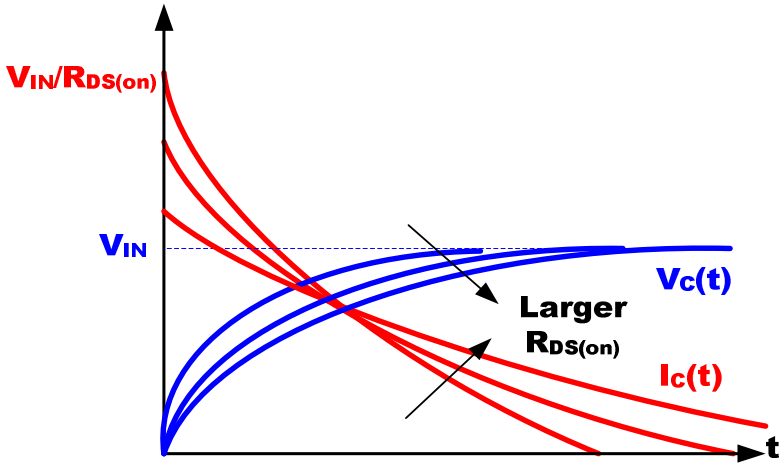

Fig. 7. Various MOSFFET R_{DS} values Vs. time

Conclusion

The users of Power MOSFET should take care to understand differences in the load switch application between various capacitors. This paper provides user design guidelines in the load switch application, and it also provides detail power and temperature calculations which can avoid MOSFET from being destroyed.

Reference

[1] R. Ericson, Fundamentals of Power Electronics, New York: Champman & Hill, 1997.
[2] Fairchild Application Note 1030
[3] International Rectifier Application Note AN-1005