Spike of Buck Converter Influenced by Reverse Recovery Current

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Introduction

Power MOSFETs have become the standard choice because of the high efficiency for the main switching devices such as Buck converter shown in Fig. 1. In Buck converter, power MOSFETs are controlled by PWM controller to achieve the target voltage and current. However, some parasitic elements of power MOSFETs could cause the operation out of SOA (safe operation area) during Buck converter working. One of the parasitic elements is the body diode whose reverse recovery current could cause a spike voltage of phase node while high side MOS turns on and low side MOS turns off. A large spike voltage might make power MOSFETs operating out of SOA and other EMI issues. This article shows the introduction of reverse recovery phenomenon and solutions to reduce the spike voltage.

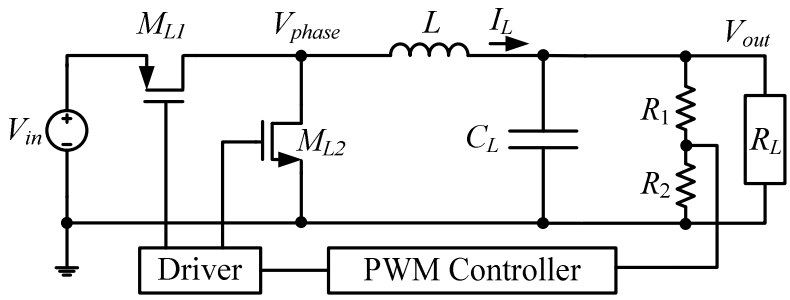

Fig. 1. Buck converter

Body Diode Reverse Recovery Time

The trench power MOSFET and the parasitic body diode is shown in Fig. 2. During power MOSFET turn-off transient, the parasitic body diode is stored minority charge and the stored charge must be removed. There are two methods to remove the excess minority charge; one is by actively negative current and the other is via recombination inside the device [1].

The total amount of excess holes (or electrons) of a p-n junction can be related to the forward current by the charge control equation [2]

$$\frac{dQ}{dt} = -\frac{Q}{\tau} + I(t) \qquad (1)$$

where Q is the total excess charges due to excess holes, and τ is the lifetime of the excess holes, and I(t) is the p-n junction current. Before t=T_0, the initial current I_F is constant in the forward conduction as shown in Fig.3. The switching beginning at t=T_0, and I(t) is determined by the external circuit. The current decreases at a constant slop C. At t=T_1, the current is zero, and then becomes negative. At t=T_2, the junction has recovered its blocking capability and the current stops to decrease. Therefore, the boundary conditions can be determined as shown in [2]

$$t \le T_0, \quad I(t) = I_F, \quad Q(0) = I_F \tau \quad \text{and} \quad T_0 \le t \le T_2, \quad I(t) = I_F - Ct, \quad T_1 = \frac{I_F}{C}$$

The solution of formula (1) can be found

$$Q(t) = Q(0)\left[\frac{\tau}{T_1}(1 - e^{\frac{-t}{\tau}}) - \frac{t}{T_1} + 1\right] \qquad (2)$$

If $T_1 >> \tau$ and according to the boundary conditions, the reverse recovery time trr can be obtained as $t_{rr} \approx \tau$ [2].

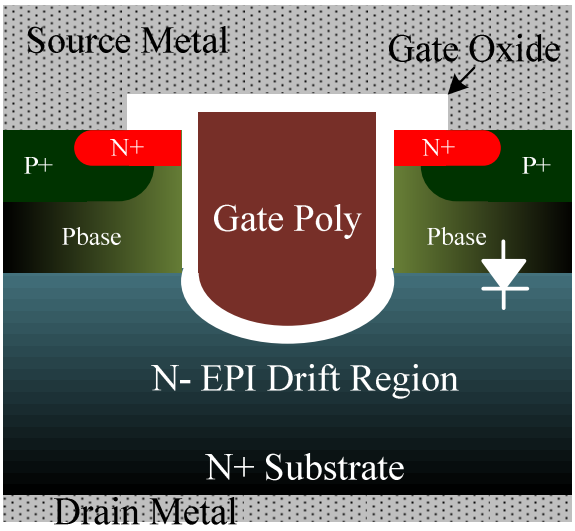

Fig. 2. Trench Power MOSFET

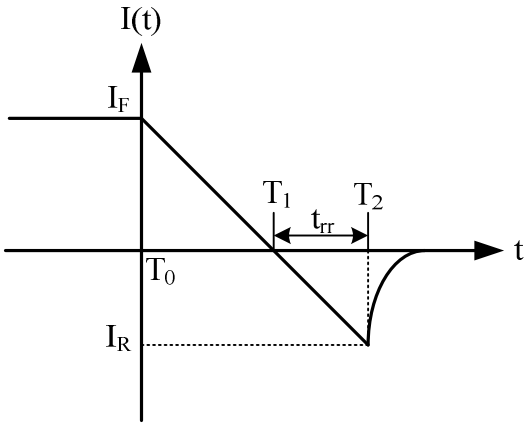

Fig. 3. Reverse Recovery Characteristics during Switching

Buck Converter Switching Analysis

Except for the reverse recovery issue, the PCB parasitic elements suck as parasitic inductances and parasitic resistances as shown in Fig.4 could influence the phase node spike.

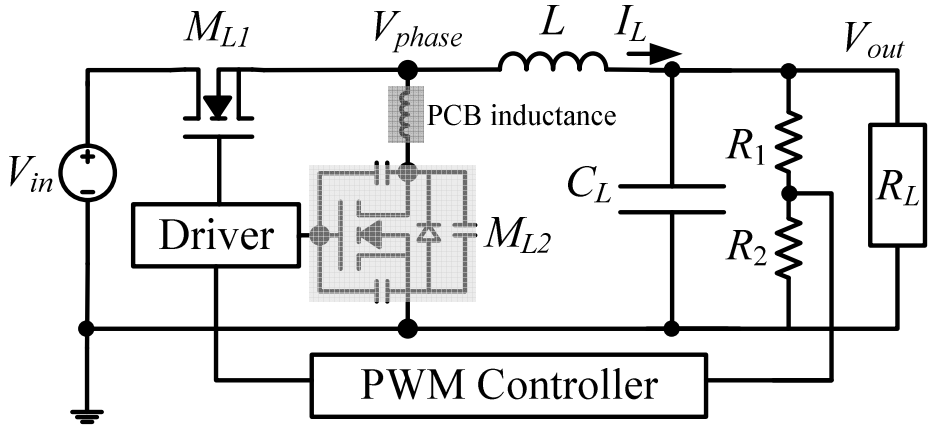

Fig. 4. Parasitic Elements in Buck Converter

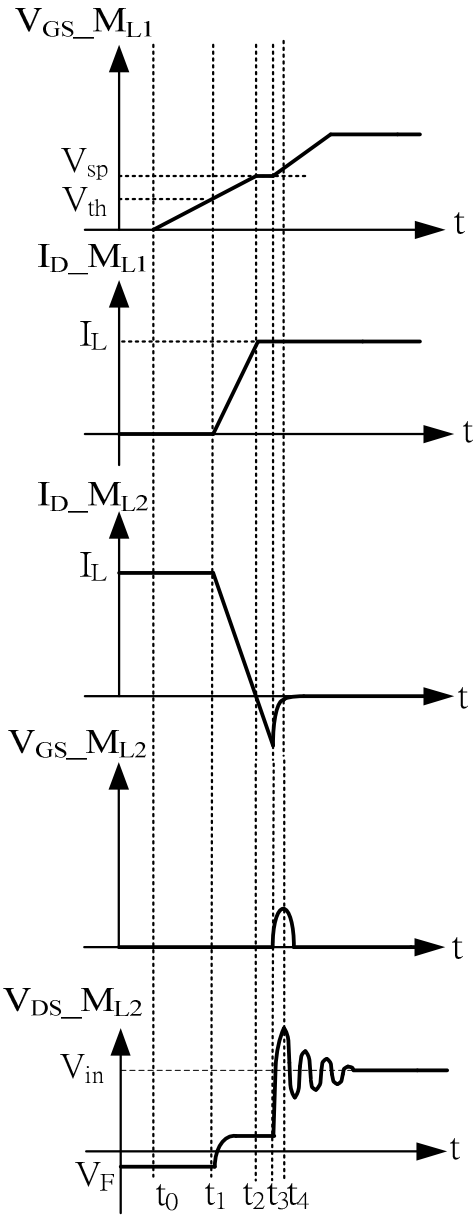

Fig. 4. Buck Converter Turn-off Transient

The analysis of turn-off transient steps can be briefly described as follows.

[$t<T_0$] High-side power MOSFET M_{L1} turns off, and Low-side power MOSFET use body diode to conduct load current.

[$T_0<t<T_1$] High-side power MOSFET starts to turn on, but the V_{GS} voltage does not reach the threshold voltage, so there is no current drawing through M_{L1}.

[$T_1<t<T_2$] The V_{GS} voltage of M_{L1} exceeds threshold voltage and it starts to conduct current, and the current of M_{L2} reduces because the sum of $I_{D\_}$ M_{L1} and $I_{D\_}$ M_{L2} equals to I_L as shown in the formula (3)

$$I_L = I_{D\_}M_{L1} + I_{D\_}M_{L2} \quad (3)$$

The current $I_{D\_}$ M_{L1} is continuous dropping until it reaches reverse recovery peak current Irr, and $I_{D\_}$ M_{L2} rises to I_L while $V_{GS\_}$ M_{L1} is Vsp, and M_{L1} operates in the saturation region. Vsp and the dropping slop of $I_{D\_}M_{L1}$ can be determined as shown in formula (4), (5), and (6).

$$V_{SP} = V_{th} + \frac{I_L}{GM} \quad (4)$$

where GM is MOSFET's transconductance, and Vth is the threshold voltage.

$$slop = \frac{dI}{dt} = \frac{I_L}{t_2 - t_1} \quad (5)$$

and

$$t_2 - t_1 = R_G \times C_{iss} \times \ell n(\frac{V_{SP}}{V_{SP} - V_{th}}) \quad (6)$$

where R_G is parasitic resistance of the gate terminal, and Ciss is parasitic capacitor seeing from the gate terminal, and I_L is the output current.

[T_2<t<T_3] In this period, the parasitic capacitor Cgd of M_{L1} starts to be charged, and the current $I_{D\_}$ M_{L1} keeps on dropping, and the PCB parasitic inductor starts to be charged. The reverse recovery starts to flow at t=T_2, and at t=T_3, the reverse recovery current reaches its peak value Irr. The stored energy in the parasitic inductor is

$$E_{LOOP} = \frac{1}{2} \times L_{PCB} \times I_{rr}^{\ 2} \quad (7)$$

where L_{PCB} is PCB parasitic inductor, and Irr is reverse recovery peak current.

The parasitic inductor keeps on being charged until the reversed body diode starts to block the voltage at t=T_3 [3].

[T_3<t<T_4] The energy stored in the parasitic PCB inductor starts to discharge, and the voltage $V_{DS\_}$ M_{L2} (phase node) rises with a high dv/dt rate. The PCB parasitic inductor forms a resonant circuit with Coss of M_{L2} and PCB parasitic resistance causing $V_{DS\_}$ M_{L2} oscillations.

Retard the Spike

Reverse recovery current pays an important role in the spike analysis. The spike voltage is caused by the energy stored in the parasitic inductor by reverse recovery current discharges and oscillated with the PCB parasitic resistance and other MOSFET's parasitic capacitors. The stored energy can be found by the formula (7). One way to reduce the spike voltage is to reduce the stored energy in the parasitic inductor. To say in other words, it means to reduce the reverse recovery peak current. The reverse recovery time can be approximately $t_{rr} \approx \tau$ as described in [2], and the larger slop can obtain the more heavy reverse recovery peak current, and the smaller slop can obtain the lighter reverse recovery peak current as shown in Fig. 5.

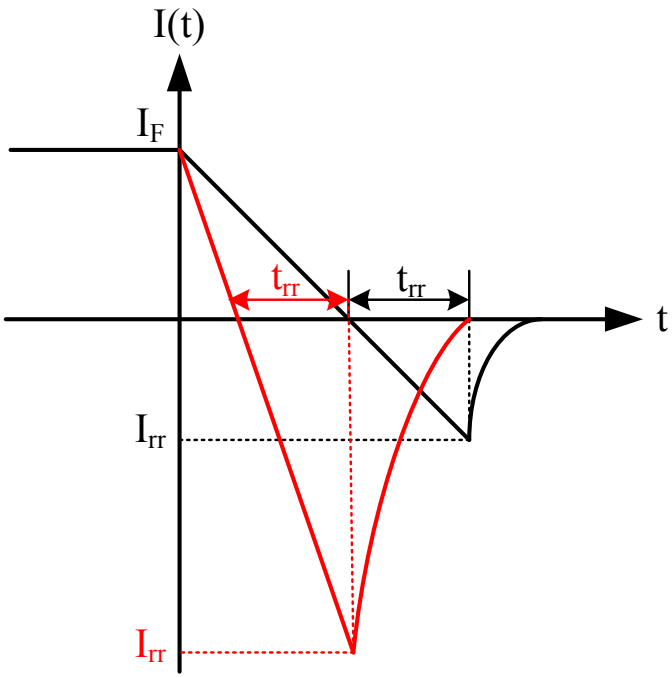

Fig. 5. Different Reverse Recovery Current in Different Slop

The reverse recovery peak current can be determined by combining reverse recovery time and the formula (5) and (6)

$$I_{rr} = \frac{dI}{dt} \times \tau = \frac{I_L}{R_G \times C_{iss} \times \ell n(\frac{V_{SP}}{V_{SP} - V_{th}})} \times \tau \qquad (8)$$

From the formula (8), if R_G and Ciss can be increased, the spike voltage could be reduced.

Experimental Results

This experiment condition is under the same controller, the same loading current and the same low-side MOSFET but different high-side MOSFET to check the spike voltage in different reverse recovery current. Experimental results are shown in Fig. 6, Fig. 7, and Fig. 8, where VIN is phase node voltage, VCC1 is high-side gate voltage, and VCC2 is low-side gate voltage. The spike voltage is the highest when high-side MOSFET is P0903BDG because of the smallest Ciss*RG factor, and the smallest spike voltage when high-side MOSFET is P0403 because of the largest Ciss*RG as shown in Table 1.

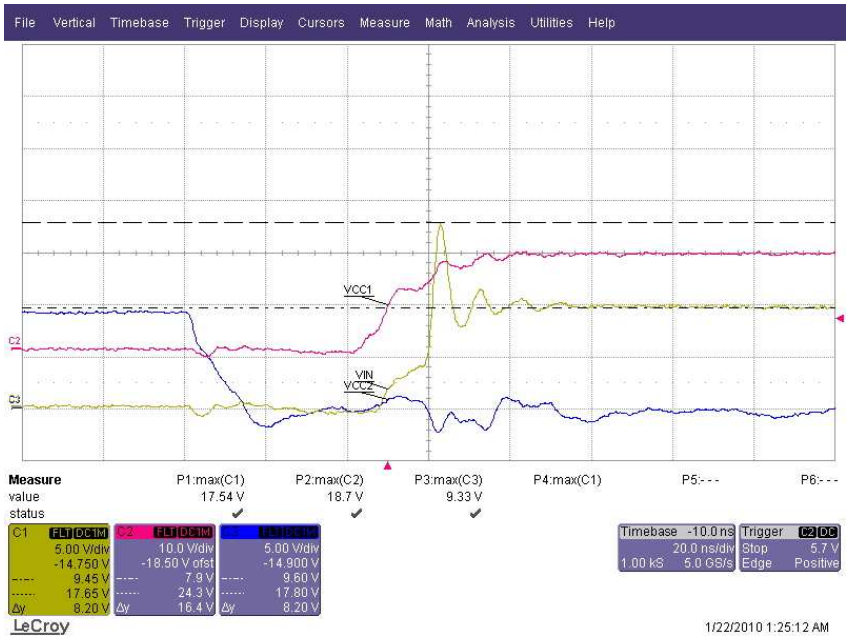

Fig. 6. Spike Voltage 8.2V with High-side MOSFET P0903BDG

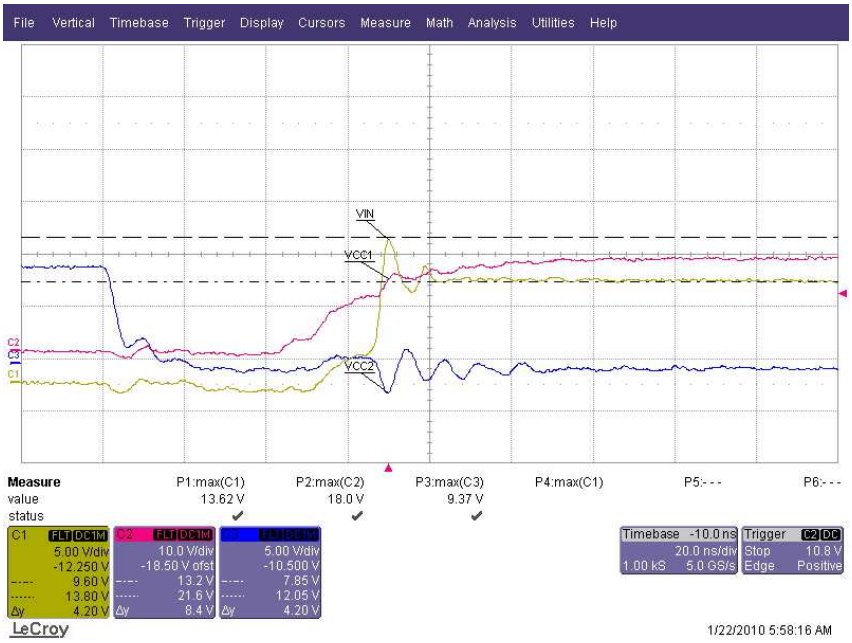

Fig. 7. Spike Voltage 4.2V with High-side MOSFET P0603BD

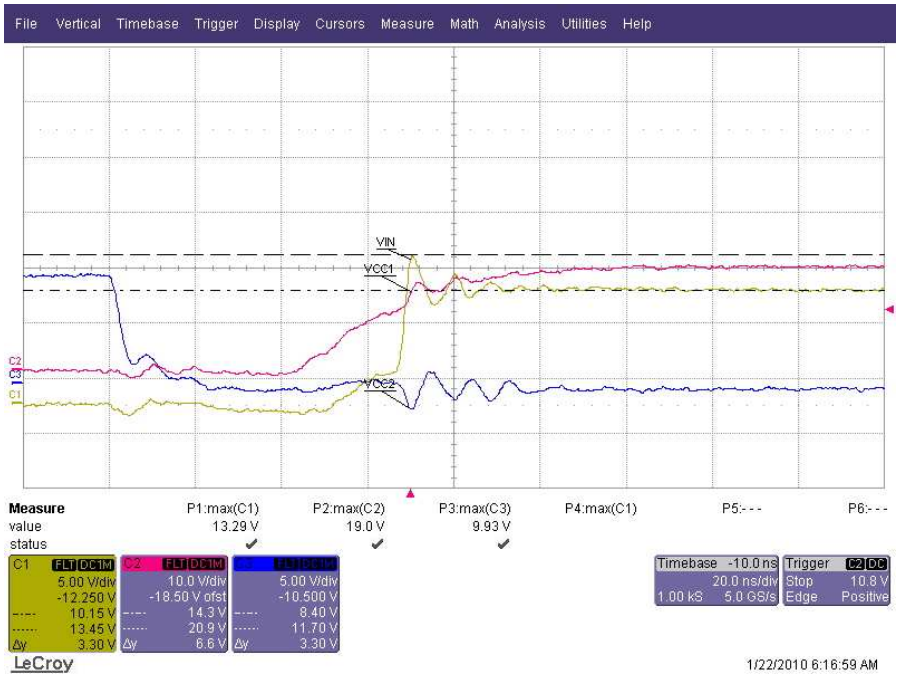

Fig. 8 Spike Voltage 3.3V with High-side MOSFET P0403BDG

Table 1. Experimental Conditions and Results

High-Side MOSFET	P0403BDG	P0603BD	P0903BDG
Ciss(PF)	2045	2407	1394
RG(Ω)	1.9	1.2	1.25
Ciss x RG	3885.5	2888.4	1742.5
Spike Voltage(V)	3.3	4.2	8.2
Load Current(A)	30	30	30

Conclusion

Spike voltage in DC-DC converters may make some drawbacks such as the EMI issues, operating out of SOA, and destroying the controller. The method to reduce the spike voltage without adding any external circuits is to increase the R_G and Ciss or to slow down the gate driver.

Reference

[1] R. Ericson, Fundamentals of Power Electronics, New York: Champman & Hill, 1997.

[2] YU C. KAO and J. R. Davis, “Correlations Between Reverse Recovery Time and Lifetime of P-N Junction Driven by a Current Ramp” *IEEE Transactions on Electron Devices*, Vol. ED-17, pp-652-657, Sep 1970.

[3] Qun Zhao and Goran Stojcic, “Characterization of Cdv/dt Induced Power Loss in Synchronous Buck DC-DC Converters” *IEEE Transactions on Power Electronics*, Vol. 22, No. 4, pp-1508-1513, July 2007.